AMENDMENTS

In the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A decoder circuit~~, which is~~ mounted on an integrated circuit[[,]] and decoding an input voltage supplied to a single external input terminal into three or more control outputs, the decoder circuit comprising:

a P-type transistor ~~in which~~ comprising an emitter (source) [[is]] connected to a power source line of a high level, a base (gate) [[is]] connected to the external input terminal[[,]] and a collector (drain) [[is]] configured to be a first [[an]] output terminal of a first control output; and

an N-type transistor ~~in which~~ comprising an emitter (source) [[is]] connected to a power source line of a low level, a base (gate) [[is]] connected to the external input terminal[[,]] and a collector (drain) [[is]] configured to be a second [[an]] output terminal of a second control output.

2. (Currently Amended) The decoder circuit according to claim 1, further comprising:

~~one or more~~ a voltage decreasing ~~means of which~~ device one end of which is connected to the external input terminal; and

~~one or more~~ a first additional transistor ~~in which~~ comprising a base (gate) [[is]] connected to ~~the other~~ another end of the voltage decreasing ~~means~~ device or to ~~one of contacts~~ a connection point of the voltage decreasing ~~means~~ device, [[and]] an emitter (source) [[is]] connected to the power source line of the high level or the low level, and a collector (drain) [[is]] configured to be a third [[an]] output terminal of a third control output.

3. (Currently Amended) The decoder circuit according to claim 1, further comprising:

a first voltage-dividing circuit~~, standing between~~ connecting the external input terminal and the base (gate) of the P-type transistor~~, in which~~ and comprising four or more voltage-dividing resistors [[are]] connected in series between the power source lines,

wherein the external input terminal is connected to a first ~~contact~~ connection point of the voltage-dividing resistors, the base (gate) of the P-type transistor is connected via a

bias resistor to a second ~~contact~~ connection point of the voltage-dividing resistors, and the base (gate) of the N-type transistor is connected via a bias resistor to a third ~~contact~~ connection point of the voltage-dividing resistors, the second ~~contact having~~ connection point is at a voltage level higher than ~~that of~~ the first ~~contact~~ connection point, and the third ~~contact having~~ connection point is at a voltage level lower than the first ~~contact~~ connection point;

~~one or more~~ a first additional transistor ~~in which~~ comprising a base (gate) [[is]] connected via a bias resistor to a ~~contact having~~ connection point of the voltage-dividing resistors at a voltage level lower than the first ~~contact~~ connection point;

a second voltage-dividing circuit to which a current ~~taken in~~ from the P-type transistor is supplied; and

~~one or more~~ a second additional transistor ~~in which~~ comprising a base (gate) [[is]] connected via a bias resistor to a ~~contact~~ connection point of voltage-dividing resistors of the second voltage-dividing circuit.

4. (Currently Amended) A photo-detecting amplifier circuit for a disk recording/reproducing apparatus, being capable of switch function by means of a decoder circuit, the photo-detecting amplifier comprising:

a decoder circuit comprising a P-type transistor and a N-type transistor and generating a first control output and a second control output; and

an amplifier receiving the first and second control outputs

~~the decoder circuit, which is mounted on an integrated circuit, decoding an input voltage supplied to a single external input terminal into three or more control outputs,~~

~~the decoder circuit comprising:~~

wherein [[a]] the P-type transistor ~~in which~~ comprises an emitter (source) [[is]] connected to a power source line of a high level, a base (gate) [[is]] connected to the external input terminal[[,]] and a collector (drain) [[is]] configured to be a first [[an]] output terminal of a first

control output[[;]], and [[an]] the N-type transistor ~~in which~~ comprises an emitter (source) [[is]] connected to a power source line of a low level, a base (gate) [[is]] connected to the external input terminal[[,]] and a collector (drain) [[is]] configured to be a second [[an]] output terminal of a second control output.

5. (Currently Amended) An optical pickup including a photo-detecting amplifier circuit for a disk recording/reproducing apparatus, being capable of switch function by means of a decoder circuit, the optical pickup comprising:

a decoder circuit comprising a P-type transistor and a N-type transistor and generating a first control output and a second control output;

an amplifier receiving the first and second control outputs and generating signals; and

an optical element responsive to one of the signals generated by the amplifier,

~~the decoder circuit, which is mounted on an integrated circuit, decoding an input voltage supplied to a single external input terminal into three or more control outputs,~~

~~the decoder circuit comprising:~~

wherein [[a]] the P-type transistor ~~in which~~ comprises an emitter (source) [[is]] connected to a power source line of a high level, a base (gate) [[is]] connected to the external input terminal[[,]] and a collector (drain) [[is]] configured to be a first [[an]] output terminal of a first control output[[;]], and [[an]] the N-type transistor ~~in which~~ comprises an emitter (source) [[is]] connected to a power source line of a low level, a base (gate) [[is]] connected to the external input terminal[[,]] and a collector (drain) [[is]] configured to be a second [[an]] output terminal of a second control output.